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	Filing Date		2006-07-19
	First Named Inventor	Dasu, Aravind R.	
	Art Unit	2193	
	Examiner Name	Bullock, Jr., Lewis Alexander Tuan Vu	
Attorney Docket Number		117316-155055	

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/VAT/	1	Fredriksson, Kimmo "Faster String Matching with Super-Alphabets" Proc of SPIRE' 2002, Lecture Notes in Computer Science 2476, pages 44-57, Springer Verlag, Berlin 2002	<input type="checkbox"/>
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/VAT/	11	Hwu, W., et al. "The Superblock: An Effective Technique for VLIW and Superscalar Compilation" Journal of Supercomputing, 7: 229-248 (1993)	<input type="checkbox"/>

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/VAT/	12	Iseli, C. et al. " A C ++ Compiler for FPGA Custom Execution Units Synthesis" IEEE Symposium on FPGAs for Custom Computing Machines, 1995	<input type="checkbox"/>
/VAT/	13	ISO/IEC JTC1/SC29/WG11 N3908 "MPEG-4 Video Verification Model version 18.0" January 2001	<input type="checkbox"/>
/VAT/	14	Jain, S., et al. "Speeding Up Program Execution Using Reconfigurable Hardware and a Hardware Function Library" VLSI Design, 1998 Proceedings, 1998 Eleventh International Conference, IEEE 1997/1998, pp. 400-405	<input type="checkbox"/>
/VAT/	15	Janssen, M., et al. " A Specification Invariant Technique for Regularity Improvement between Flow-Graph Clusters" IEEE Proceedings of the 1996 European Design and Test Conference (ED&TC), pages 138-143 (1996)	<input type="checkbox"/>
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/VAT/	18	Kasahara, H., et al. " Practical Multiprocessor Scheduling Algorithms for Efficient Parallel Processing" IEEE Trans. On Comp., V33, Nul 1, 1984, 1023-1029	<input type="checkbox"/>
/VAT/	19	Kastner, R. et al."Instruction Generation for Hybrid Reconfigurable Systems" International Conference on Computer-Aided Design (ICCAD), November, 2001	<input type="checkbox"/>
/VAT/	20	Kastrup, B. et al. "ConCiSe: A Compiler-Driven CPLD-Based Instruction Set Accelerator" IEEE Symposium on Field Programmable Custom Computing Machines, 1999	<input type="checkbox"/>
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/VAT/	23	Kuramochi, M., et al. "An Efficient Algorithm for Discovering Frequent Subgraphs" Technical Report 02-026, University of Minnesota, 2002	<input type="checkbox"/>
/VAT/	24	Kwok, Y.K., et al. "Dynamic Critical-Path Scheduling: An Effective Technique for Allocating Task Graphs to Multiprocessors" IEEE Transactions on Parallel and Distributed Systems, Vol. 7, NO 5, May 1996 pp. 506-521	<input type="checkbox"/>
/VAT/	25	Lai, Y.T., et al. "Hierarchical Interconnection Structures for Field Programmable Gate Arrays" IEEE Transactions on Very Large Scale Integration (VLSI) Systems, Vol. 5, No 2, pp. 186-196, June 1997	<input type="checkbox"/>
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/VAT/	27	Lee, W. et al. "Space-Time Scheduling of Instruction-Level Parallelism on a Raw Machine", Proc of the Eighth International Conference on Architectural Support for Programming Languages and Operating Systems (ASPLOS), San Jose, CA, October 1998	<input type="checkbox"/>
/VAT/	28	Li, S., et al. "Configuration Code Generation and Optimizations for Heterogeneous Reconfigurable DSPs" Proceedings of SIPSS99	<input type="checkbox"/>
/VAT/	29	Li, W., et al. "Routability Prediction for Hierarchical FPGAs" Ninth Great Lakes Symposium on VLSI, pp. 256-259, 4-6 March 1999	<input type="checkbox"/>
/VAT/	30	Liu, J. et al. "Variable Instruction Set Architecture and Its Compiler Support" IEEE Transactions on Computers, 2003	<input type="checkbox"/>
/VAT/	31	Marquardt, A. et al. "Using Cluster-Based Logic Blocks and Timing-Driven Packing to Improve FPGA Speed and Density" Proceeding of the 1999 ACM/SIGDA Seventh International Symposium on Field Programmable Gate Arrays, p. 37-46, February 21-23, 1999, Monterey	<input type="checkbox"/>
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/VAT/	34	Mirsky, E. et al. " MATRIX: A Reconfigurable Computing Architecture with Configurable Instruction Distribution and Deployable Resources" IEEE Symposium on FPGAs for Custom Computing Machines, April 17-19, 1996, Napa, CA	<input type="checkbox"/>
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/VAT/	41	Perchant, A., et al. " A New Definition for Fuzzy Attributed Graph Homomorphism with Application to Structural Shape Recognition in Brain Imaging" hi IMTC'99, 16th IEEE Instrumentation and Measurement Technology Conference, pages 1801-1806 Venice, Italy, May, 1999	<input type="checkbox"/>
/VAT/	42	Rabaey, Jan M. "Reconfigurable Processing: The Solution to Low-Power Programmable DSP" Proceedings 1997 ICASSP Conference Munich April 1997	<input type="checkbox"/>
/VAT/	43	Rangarajan, A., et al. " A Lagrangian Relaxation Network for Graph Matching" IEEE Transactions on Neural Networks, 7 (6): 1365-1381, 1996	<input type="checkbox"/>
/VAT/	44	Rao, D., et al. "On Clustering for Maximal Regularity Extraction" IEEE Transactions on Computer-Aided Design, Vol. 12, No. 8, August, 1993	<input type="checkbox"/>

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/VAT/	45	Rewini, H., et al. "Static Scheduling of Conditional Branches in Parallel Programs" Journal of Parallel and Distributed Computing, 24, 4154 (1995)	<input type="checkbox"/>
/VAT/	46	Reyner, Steven W. " An Analysis of a Good Algorithm for the Subtree Problem" SIAM Journal of Computing, 6 (4): 730-732, 1997	<input type="checkbox"/>
/VAT/	47	Sarrigeorgidis, K., et al. "Massively Parallel Wireless Reconfigurable Processor Architecture and Programming" IOTiz Reconfigurable Architectures Workshop, Nice, France, April 22, 2003	<input type="checkbox"/>
/VAT/	48	Sawitzki, S. et al. "CoMPARE: A Simple Reconfigurable Processor Architecture Exploiting Instruction Level Parallelism" Proc. Of PART, pp.213-224, Springer-Verlag, 1998	<input type="checkbox"/>
/VAT/	49	Schoner, B., et al. " Issues in Wireless Video Coding using Run-Time-reconfigurable FPGAs" Proc of the IEEE Symposium on FPGAs for Custom Computing Machines, Napa CA, April 19-21, 1995	<input type="checkbox"/>
/VAT/	50	Singh, A., et al. " Efficient circuit Clustering for Area and Power Reduction in FPGAs" ACM Transactions on Design Automation of Electronic Systems, Volume 7, Issue 4, October 2002, pp. 643-663	<input type="checkbox"/>

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